In the Specification

Amend the specification as follows:

Amend the paragraph beginning at page 1 line 20 as follows:

Overlay measurement determines the relative positioning errors among patterns on the same or different layers subsequent to the lithographic patterning process. Overlay measurement is critical to achieving the nanometer-scale positioning of patterns across multiple process layers necessary for advanced semiconductor manufacturing. Successful overlay ~~refers to~~ refers to a condition where the relative locations of patterns throughout the sequence of manufactured layers that comprise the finished circuit correspond to the desired circuit design within allowed tolerances. Currently, overlay measurement is performed using targets comprised of nested sub-patterns printed together with the functional circuit elements at each successive lithographic step. Images of the overlay targets are captured by an imaging system. Algorithms applied to the captured images extract the relative displacement of the nested sub-patterns. The resulting overlay error is typically expressed as the vector sum of the (x, y) components of the relative displacement.

Amend the paragraph beginning at page 5 line 19 as follows:

The first and second grid patterns may be formed on the same or different lithographic layers of an electronic substrate, and where a plurality ~~second~~ of second grid patterns are used, they may each be formed on different lithographic layers of an electronic substrate.

Amend the paragraph beginning at page 8 line 10 as follows:

In a further aspect, the present invention is directed to a metrology tool system comprising a plurality of metrology tools. Each metrology tool comprises a stage for securing a lithographically produced semiconductor substrate, an energy source, a lens for directing the energy source onto a surface of the substrate, a lens for capturing an image of a structure lithographically produced on the substrate, and an image processor for measuring distance between points on the image of the lithographically-produced structure on the substrate. Additionally, each metrology tool stage includes an alignment target affixed thereto comprising a contrasting set of elements forming a grid pattern having a plurality of grid segments in the at least one of the x and y directions, each grid segment having a distance between elements equal to the same period. Each metrology tool is adapted to be calibrated by measuring the period of the grid segments in the grid pattern on the alignment target ~~associated~~ affixed to the tool stage.

Amend the paragraph beginning at page 12 line 22 as follows:

The preferred embodiment of the target of the present invention shown ~~in Fig 2.~~ in Fig. 2 is comprised of a 3 x 3 array of reference grid and 8 x 8 array of sub-grids. Centrally located at frame address (0,0) is a reference sub-grid 24 printed simultaneously with the reference grid 22. Around the reference sub-grid are eight equally spaced post sub-grids 24 printed at simultaneous or subsequent lithography steps. The lithography steps that print a sub-grid can be at the same layer or different layers of the manufacturing process as any other sub-grid. Each sub-grid is designed to be centered within the frame of a reference grid of known major period *D*. The sub-grids may be arrays of horizontally and vertically oriented features (e.g., lines or spaces, line or space segments, or contact holes to maintain compatibility with the layer ground-rules) at a

known minor period p that can be resolved by the imaging tool, but is much smaller than D. Examples of the elements that may be used to form the sub-grids, or the reference grids, are shown in Figs. 3a, 3b and 3c. In Fig. 3a, sub-grid 24a is comprised of solid lines (or spaces on a solid background) that intersect to form the individual subframes in an 8 x 8 array. In Fig. 3b, sub-grid 24b is composed of lines or spaces that do not intersect, yet still form the substantial outlines of the subframes. The lines or spaces of that make up the elements of sub-grid 24b (or sub-grid 24a) may themselves be arrays of equally spaced parallel lines oriented either parallel (24") or perpendicular (24') to the direction of the element. As shown in Fig. 24c, the elements may be composed of holes to form the array.

Amend the paragraph beginning at page 21 line 9 as follows:

A general flowchart of the overlay error extraction method that we have examined in the example above, is shown in Fig. 14. In the first step 102, the target image is scanned in the x- and y-directions to produce a digitized target image I (x, y) with a pixel size much smaller than the magnified sub-grid period M x p. The (x, y) scanned intensities are ~~than~~ then integrated 104 into intensities I_n (x) and I_m (y). The integrated intensities are then separated 106 into single frame intensities I_{nm} (x) and I_{nm} (y). The single frame intensities are then aligned 108 using reference signals I_R (x) and I_R (y) common to each target frame. The I_F (x) and I_F (y) intensities are then fit 110 to sinusoids in each frame to determine the parameters A, B, d and s, where parameter d is the ratio of pixel size c to sub-grid period p and parameter s measures the center of the sinusoidal patterns.